WHAT IS CLAIMED IS:

1. A method for flip-chip bonding an integrated circuit die to a substrate, comprising the steps of:

providing said integrated circuit die with at least one gold bump,

forming a barrier layer on said gold bump,

forming a bronzing agent on said barrier layer, and

providing said substrate with at least one conductive bonding area, said bonding area covered with gold.

2. The method of claim 1 further comprising exposing said bronzing agent to a plasma comprising fluorine such that fluorine-containing compounds form on said bronzing agent so as to allow wetting to occur.

3. The method of claim 1, wherein said gold bump comprises at least about 90 weight % Au, said barrier layer comprises at least about 90 weight % Ni, and said bronzing agent comprises about 100 weight % Pb.

4. The method of claim 1, wherein said bronzing agent comprises a lead-indium alloy.

5. The method of claim 1, wherein said bronzing agent comprises pure indium.

6. The method of claim 1 further comprising depositing a film of gold on said bronzing agent so as to prevent oxidation of said bronzing agent.

7. The method of claim 1 further comprising depositing a

film of platinum on said bronzing agent so as to prevent oxidation of said bronzing agent.

8. The method of claim 1 further comprising:

aligning said bronzing agent of said integrated circuit die on said conductive bonding area of said substrate;

providing a compression force so as to establish contact between said bronzing agent of said integrated circuit die and said conductive bonding area of said substrate; and

alloying said bronzing agent on said integrated circuit die such that said bronzing agent and said gold on said conductive bonding area of said substrate form an intermetallic compound.

9. The method of claim 8, wherein said alloying comprises:

subjecting said integrated circuit die and said substrate to a background temperature while maintaining said compression force, said background temperature sufficient to allow said bronzing agent to yield, said compression force sufficient to deform said bronzing agent at said background temperature;

allowing said bronzing agent to yield;

maintaining the distance between said gold bump and said conductive bonding pad; and

subjecting said integrated circuit die and said substrate to a bonding temperature.

10. The method of claim 9, wherein said barrier layer

prevents said gold bump from diffusing into said bronzing agent during said alloying process.

11. The method of claim 8, wherein said intermetallic compound is a AuPb2.

12. The method of claim 9, wherein when subject to said bonding temperature during said alloying process, said intermetallic compound enters a liquid state such that upon cooling a hermetic bond is formed.

13. The method of claim 9, wherein said compression force is greater than the yield limit of said bronzing agent and less than the yield limit of said gold bump.

14. The method of claim 13 wherein allowing said bronzing agent to yield adjusts the height of the combination of said gold bump and said barrier layer by deforming said bronzing agent.

15. The method of claim 8, wherein the compression force ranges from about 0.03 to about 0.2 N per gold bump.

16. A method for flip-chip bonding an integrated circuit die to a substrate, comprising the steps of:

providing said integrated circuit die with a first gold bump;

forming a first barrier layer on said first gold bump;

forming a bronzing agent on said barrier layer;

providing said substrate with a conductive bonding area comprising a second gold bump;

forming a second barrier layer on said conductive

bonding area; and

forming a gold layer on said second barrier layer.

17. The method of claim 16 further comprising exposing said bronzing agent to a plasma comprising fluorine containing species such that fluorine-containing compounds form on said bronzing agent so as to allow wetting to occur.

18. The method of claim 16, wherein said first and second gold bumps comprise at least about 90 weight % Au, said first and second barrier layers comprise at least about 90 weight % Ni, and said bronzing agent comprises about 100 weight % Pb.

19. The method of claim 16, wherein said bronzing agent comprises a lead-indium alloy.

20. The method of claim 16, wherein said bronzing agent comprises pure indium.

21. The method of claim 16 further comprising depositing a film of gold on said bronzing agent so as to prevent oxidation of said bronzing agent.

22. The method of claim 16 further comprising depositing a film of platinum on said bronzing agent so as to prevent oxidation of said bronzing agent.

23. The method of claim 16 further comprising:

aligning said bronzing agent of said integrated circuit die on said gold layer disposed on said second barrier layer;

providing a compression force so as to establish contact between said bronzing agent of said integrated circuit

die and said gold layer disposed on said second barrier layer; and

alloying said bronzing agent of said integrated circuit die such that said bronzing agent and said gold layer disposed on said second barrier layer form an intermetallic compound.

24. The method of claim 23, wherein said alloying comprises:

subjecting said integrated circuit die and said substrate to a background temperature while maintaining said compression force, said background temperature sufficient to allow said bronzing agent to yield, said compression force sufficient to deform said bronzing agent at said background temperature;

allowing said bronzing agent to yield;

maintaining the distance between said first gold bump and said second gold bump; and

subjecting said integrated circuit die and said substrate to a bonding temperature.

25. The method of claim 24, wherein said first barrier layer prevents said first gold bump from diffusing into said bronzing agent during said alloying process.

26. The method of claim 24, wherein said second barrier layer prevents the second gold bump from diffusing into the bronzing agent during said alloying process.

27. The method of claim 23, wherein said intermetallic

compound is a AUPb2.

28. The method of claim 24, wherein when subject to said background temperature during said alloying process, said intermetallic compound enters a liquid state such that upon cooling a hermetic bond is formed.

29. The method of claim 24, wherein said compression force is greater than the yield limit of said bronzing agent and less than the yield limit of said first and second gold bumps.

30. The method of claim 29, wherein allowing said bronzing agent to yield adjusts the distance separating the integrated circuit die and the substrate by deforming said bronzing agent.

31. The method of claim 23, wherein the compression force ranges from about 0.03 to about 0.20 N grams per bond being formed.

32. A flip-chip structure comprising:

an integrated circuit die comprising a gold bump,

a barrier layer formed on said gold bump,

a bronzing agent formed on said barrier layer, and

a substrate comprising at least one conductive bonding area corresponding to said gold bump, said bonding area covered with gold.

33. The flip-chip structure of claim 32, wherein said gold bump comprises at least about 90 weight % Au, said barrier layer comprises at least about 90 weight % Ni, and said bronzing agent comprises about 100 weight % Pb.

34. The flip-chip structure of claim 32, wherein said bronzing agent comprises a lead-indium alloy.

35. The flip-chip structure of claim 32, wherein said bronzing agent pure indium.

36. The flip-chip structure of claim 32, wherein the bronzing agent is coated with a film of gold so as to prevent oxidation of said bronzing agent.

37. The flip-chip structure of claim 32, wherein the bronzing agent is coated with a film of platinum so as to prevent oxidation of said bronzing agent.

38. The flip-chip structure of claim 32, wherein said barrier layer prevents said gold bump from diffusing into said bronzing agent.

39. A flip-chip bond comprising:

an integrated circuit die comprising a gold bump;

a barrier layer formed on said gold bump;

a substrate comprising at least one conductive bonding area corresponding to said gold bump, said bonding area covered with gold; and

an intermetallic compound which forms a bond between said barrier layer and said conductive bonding area.

40. A flip-chip structure comprising:

an integrated circuit die comprising a first gold bump;

a first barrier layer formed on said first gold bump;

a bronzing agent formed on said first barrier layer;

a substrate having a conductive bonding area comprising a second gold bump;

a second barrier layer formed on said conductive bonding area; and

a gold layer formed on said second barrier layer.

41. The flip-chip structure of claim 40, wherein said first and second gold bumps comprise at least about 90 weight % Au, said first and second barrier layers comprise at least about 90 weight % Ni, and said bronzing agent comprises about 100 weight % Pb.

42. The flip-chip structure of claim 40, wherein said bronzing agent comprises a lead-indium alloy.

43. The flip-chip structure of claim 40, wherein said bronzing agent comprises pure indium.

44. The flip-chip structure of claim 40, wherein the bronzing agent is coated with a film of gold so as to prevent oxidation of said bronzing agent.

45. The flip-chip structure of claim 40, wherein the bronzing agent is coated with a film of platinum so as to prevent oxidation of said bronzing agent.

46. The flip-chip structure of claim 40, wherein said first barrier layer prevents said first gold bump from diffusing into said bronzing agent.

47. The flip-chip structure of claim 40, wherein said second barrier layer prevents the second gold bump from diffusing

into the bronzing agent.

48. A flip-chip bond comprising:

an integrated circuit die comprising a first gold bump;

a first barrier layer formed on said first gold bump;

a substrate having a conductive bonding area comprising a second gold bump;

a second barrier layer formed on said conductive bonding area; and

an intermetallic compound which forms a bond between said first barrier layer and said second barrier layer.

49. A method for forming a hermetic seal between an integrated circuit die and a substrate, comprising the steps of:

providing said integrated circuit die with a first continuous gold band;

forming a barrier layer on said gold band;

forming a bronzing agent on said barrier layer; and

providing said substrate with a second continuous gold band, said second gold band being substantially the mirror image of said first gold band.

50. The method of claim 49 further comprising:

aligning said bronzing agent on said second gold band on said substrate;

providing a compression force so as to establish contact between said bronzing agent and said second gold band on said substrate; and

alloying said bronzing agent such that said bronzing agent and said second gold band on said substrate form a hermetic seal between said integrated circuit die and said substrate.

51. The method of claim 50, wherein said hermetic seal comprises an intermetallic compound, $AuPb_2$.

52. A method for forming a hermetic seal between an integrated circuit die and a substrate, comprising the steps of:

providing said integrated circuit die with a first continuous gold band;

forming a barrier layer on said gold band;

forming a bronzing agent on said barrier layer;

providing said substrate with a second continuous gold band, said second gold band being substantially the mirror image of said first gold band;

forming a second barrier layer on said second gold band; and

forming a third continuous gold band on said second barrier layer.

53. The method of claim 52 further comprising:

aligning said bronzing agent on said third gold band on said substrate;

providing a compression force so as to establish contact between said bronzing agent and said third gold band on said substrate; and

alloying said bronzing agent such that said bronzing

agent and said third gold band on said substrate form a hermetic seal between said integrated circuit die and said substrate.

54. The method of claim 53, wherein said hermetic seal comprises an intermetallic compound, AuPb2.